



## **Section 10**

### **Physical Dimensions/ Appendices**





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## TapePak®

The latest generation in VLSI packaging, TapePak is the package of the future—low-cost, reliable, high-leadcount packaging that's easy to handle, easy to test, and easy to mount. It's also compatible with existing surface-mount technology.

TapePak uses tape-automated bonding technology and a unique, patented outer ring to protect the leads and, at the same time, provide an effective test interface.

This outer ring is molded at the same time as the body of the package and creates test points outside the package leads. The test ring is discarded along with the tape as the package is excised by the automatic pick-and-place machine at the point of assembly.

During testing, the leads themselves never come in contact with the test socket, so lead damage and coplanarity problems are eliminated. The test ring also allows burn-in to be performed on each device.

Not only does this ring protect the leads during handling, testing and assembly, but it also allows leads to be placed on centers of 0.012 inch–0.020 inch (0.3 mm–0.5 mm), while the test points are placed on standard centers of 0.020 inch (0.5 mm), 0.025 inch (0.65 mm) or 0.050 inch (1.27 mm). That way, the test points are compatible with existing automatic test equipment.

TapePak packages are significantly smaller than conventional and alternative surface-mount packages. TapePak lead counts range from 40 to greater than 360, yet the largest package measures only 1.1 inches (28 mm) square.

**Comparison of TapePak and Conventional Packages**

	40L DIP	44L PLCC	40L TapePak			
Lead thickness (mils)	10.0	10.0	2.8			
Lead pitch (mils)	100	50	20			
Package length (mils)	2050	650	350			
Package width (mils)	600	650	350			
Package thickness (mils)*	175	180	71			
Volume ratio	24.4	9.1	1			
	40L DIP	44L PLCC	40L TapePak			
	Long	Short	Long	Short	Long	Short
Lead length (in)	1.0	0.3	0.35	0.25	0.1	0.1
Resistance (mOhm)	7	4	4	3	2.4	2.4
Inductance (nH)	22	6.0	6.5	5	1.2	1.2
Capacitance (pF) (lead to lead)	0.5	0.2	0.3	0.2	0.2	0.1

\*Measured from seating plane to the top of the package.

A TapePak device can be less than 1/10 the size of a traditional DIP and 1/3 the size of other surface-mount packages such as a PLCC.

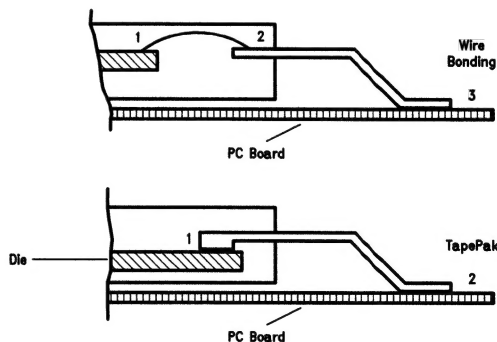
TapePak technology was designed to take full advantage of automatic assembly systems with their high speed and precision. It can be used with existing precision surface-mount assembly equipment with minimal modification. The only requirement is an accessory for removing the test ring and forming the leads at the point of assembly.

TapePak also provides a significant improvement in the electrical characteristics of each package. Lead capacitance and inductance, for example, can be reduced up to ten times that of other packages. Signal propagation time is also reduced, and thermal characteristics are improved. Because of the tremendous space savings, TapePak technology offers much greater power density per unit area as compared to DIP or alternative surface-mount packages.

Performance and reliability are improved because there are one-third fewer connections between the die and the PC board. Low-stress molding compounds also improve package reliability. TapePak devices pass stringent environmental tests, including autoclaving at 121°C at 15 psi and thermal shock from -65°C to +150°C for 1000 cycles.

No other package takes similar advantage of materials technology to provide the combination of low cost, high density, testability, damage resistance, and reliability.

TapePak has been accepted as an industry standard by the Joint Electronic Device and Engineering Council (JEDEC) and registration is in progress with the Electronic Industries Association of Japan (EIAJ). TapePak technology has also been licensed to other manufacturers for their own proprietary devices.



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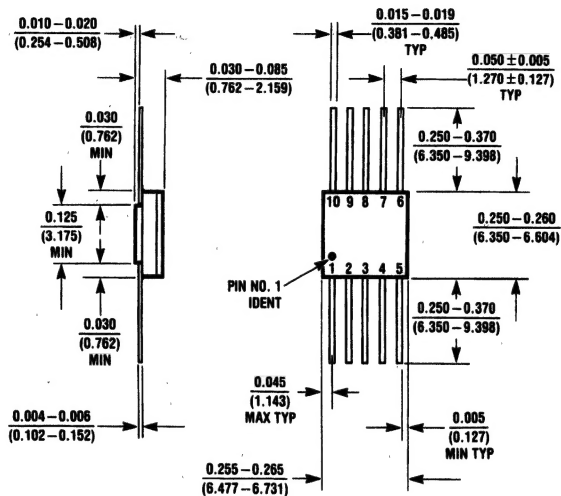
**With TapePak, there are one-third fewer connections between die and board than with traditional wire bonding.**





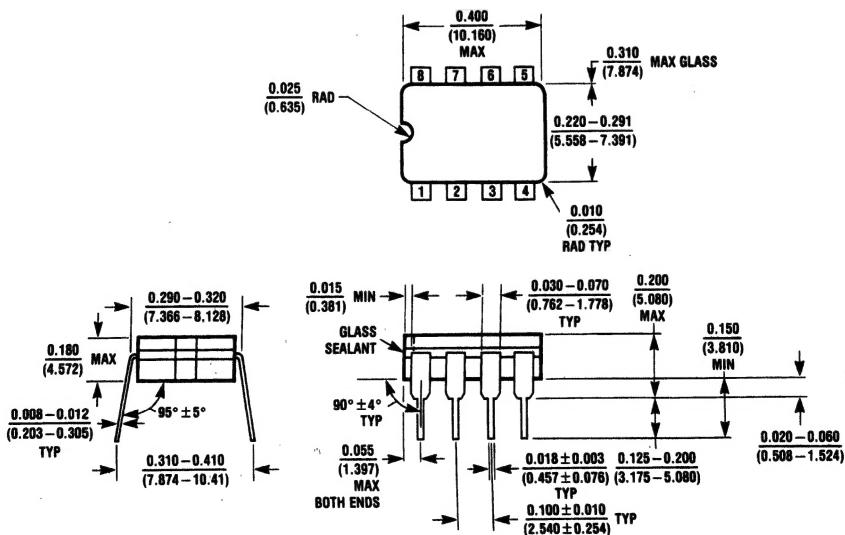
All dimensions are in inches (millimeters)

## 10 Lead Ceramic Flatpack Package (F) NS Package Number F10B



F10B (REV F)

## 8 Lead Ceramic Dual-In-Line Package (J) NS Package Number J08A



J08A (REV J)



**24 Lead Ceramic Dual-In-Line Package (J)  
NS Package Number J24F**

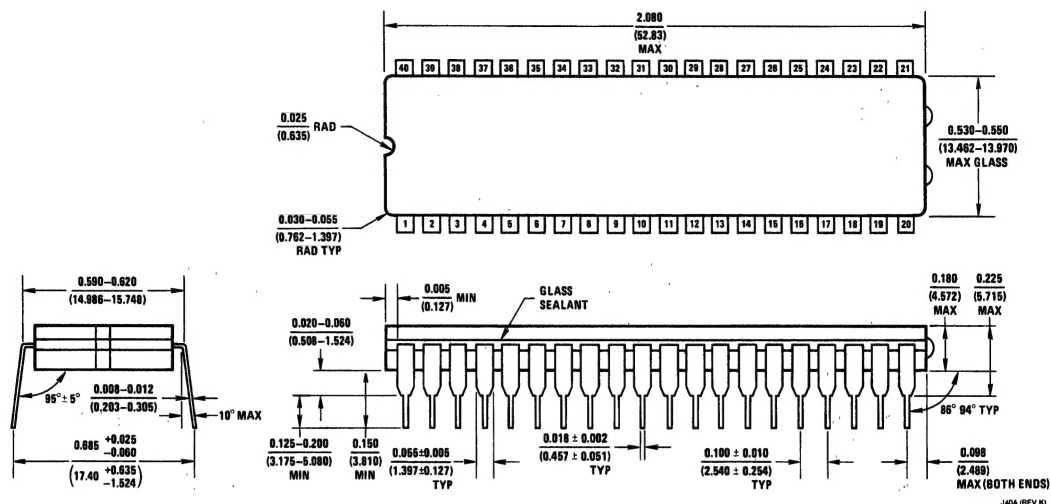


**28 Lead Ceramic Dual-In-Line Package (J)  
NS Package Number J28A**

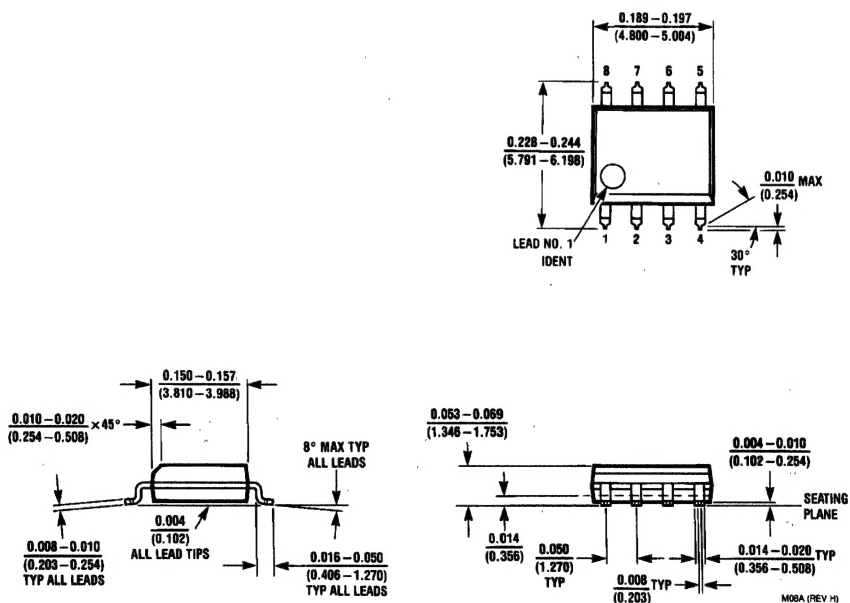




## 40 Lead Ceramic Dual-In-Line Package (J) NS Package Number J40A

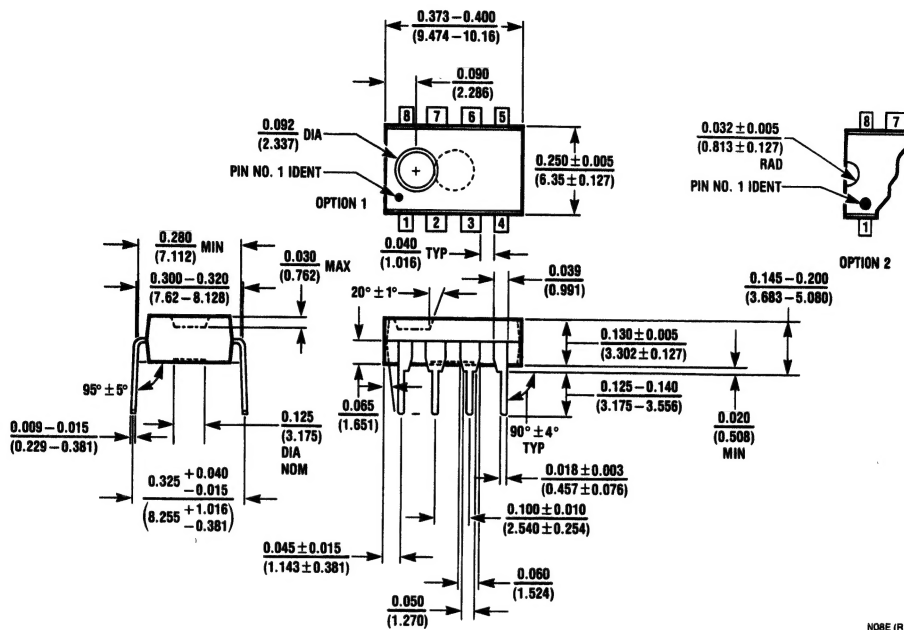


## 8 Lead (0.150" Wide) Molded Small Outline Package (M) NS Package Number M08A

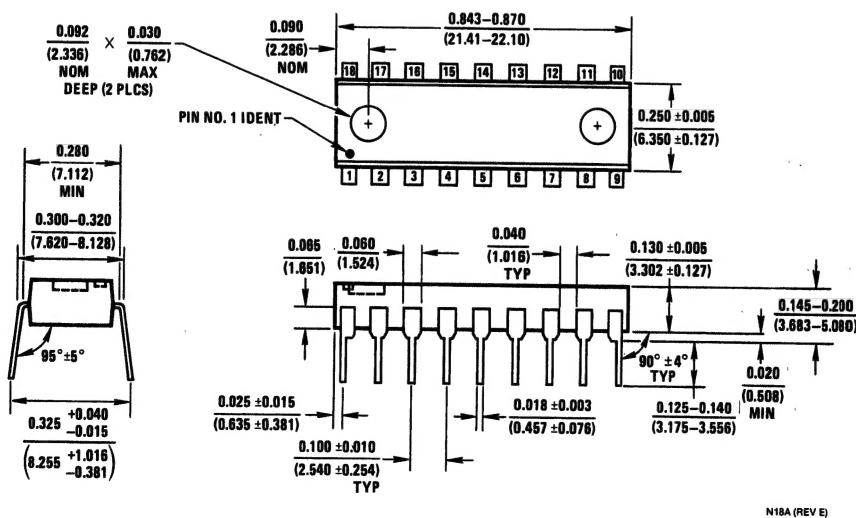




# 8 Lead Molded Dual-In-Line Package (N) NS Package Number N08E

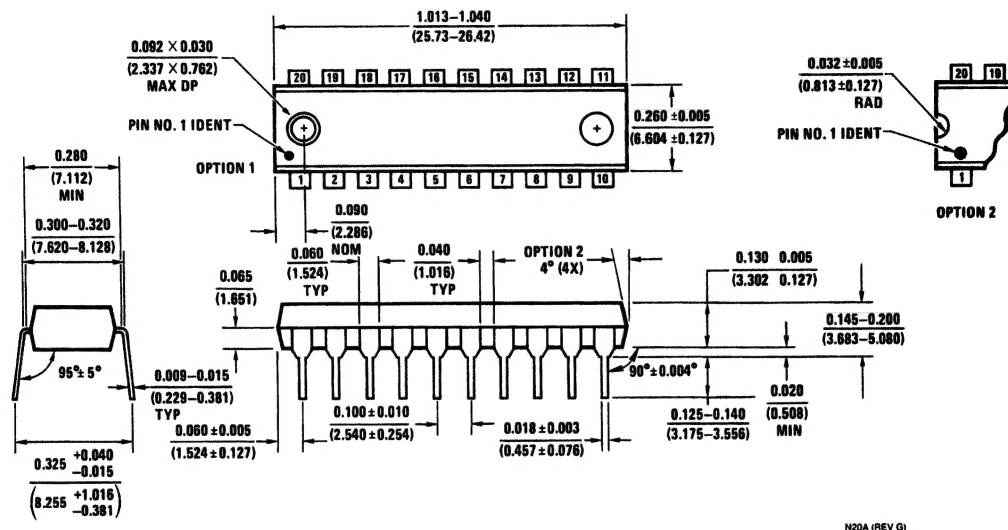


# 18 Lead Molded Dual-In-Line Package (N) NS Package Number N18A

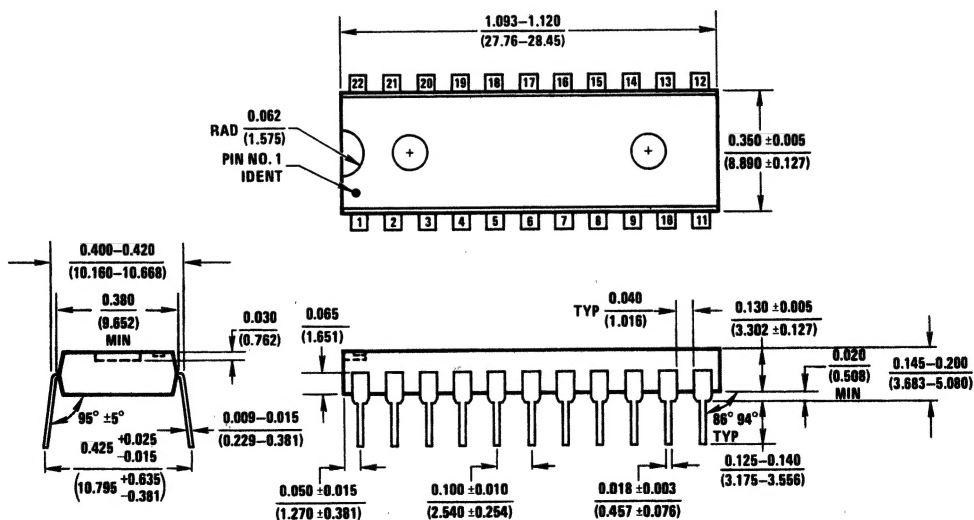




## 20 Lead Molded Dual-In-Line Package (N) NS Package Number N20A

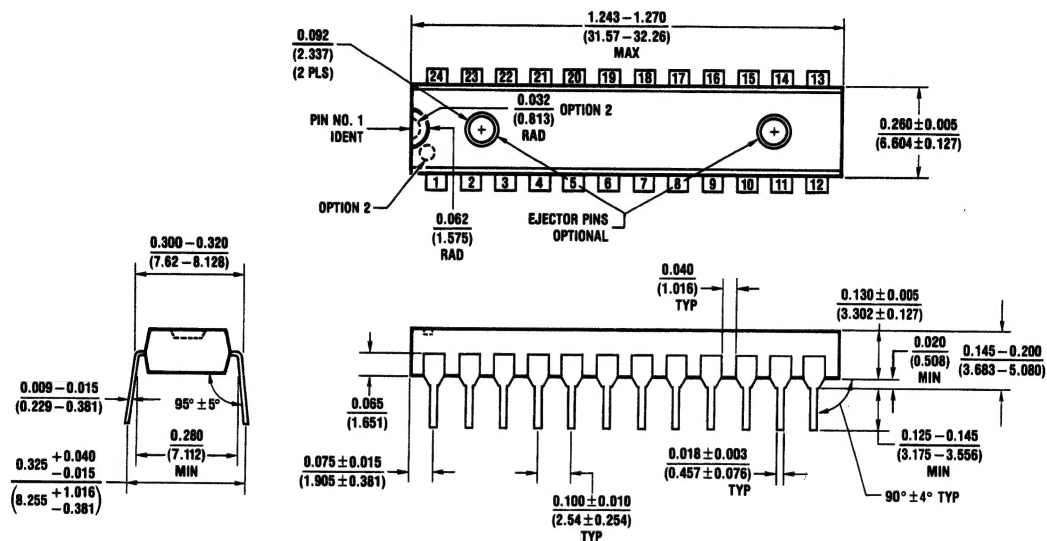


## 22 Lead Molded Dual-In-Line Package (N) NS Package Number N22A



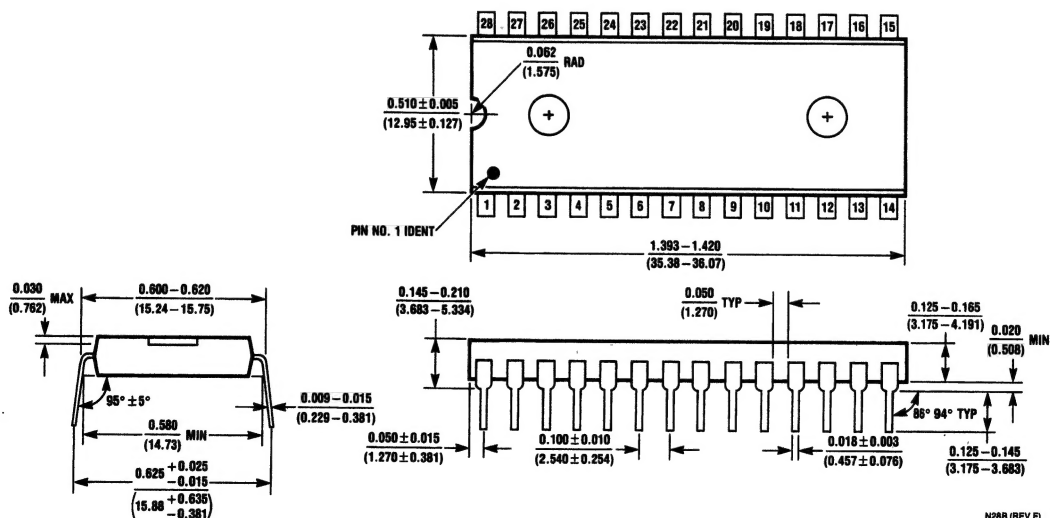


## 24 Lead Skinny Dual-In-Line Package (0.300" Centers Molded) (N) NS Package Number N24C



N24C (REV F)

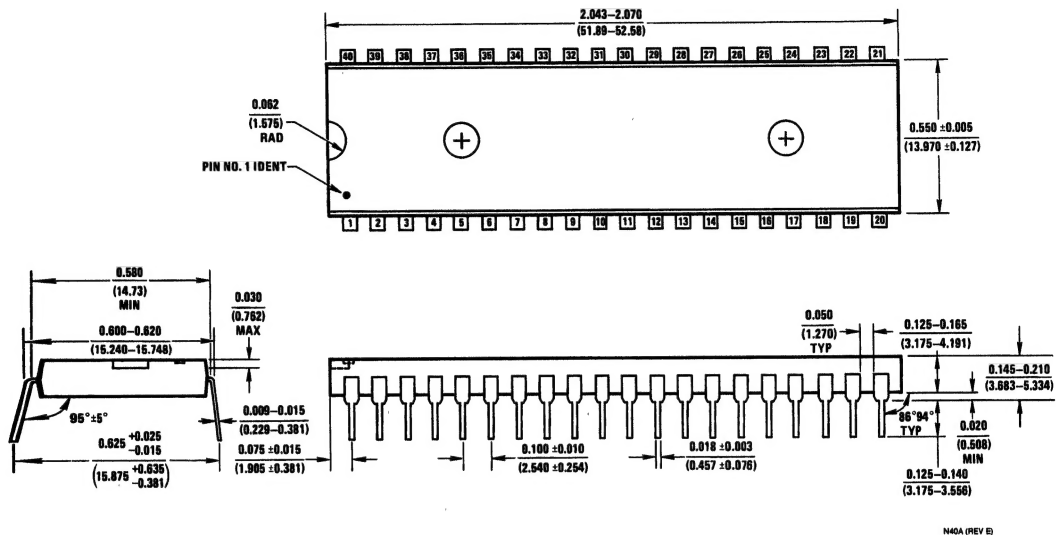
## 28 Lead Molded Dual-In-Line Package (N) NS Package Number N28B



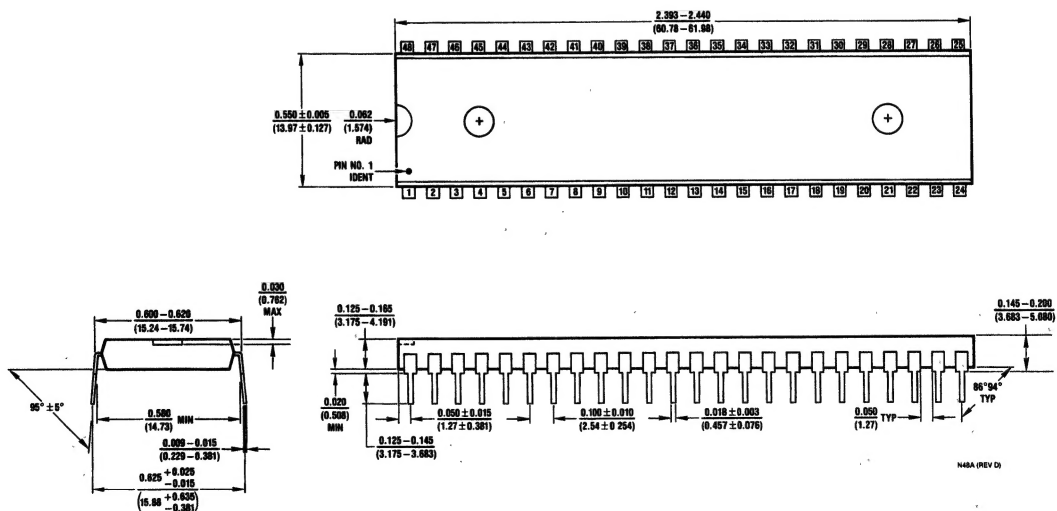
N28B (REV E)



## 40 Lead Molded Dual-In-Line Package (N) NS Package Number N40A



## 48 Lead Molded Dual-In-Line Package (N) NS Package Number N48A





## Physical Dimensions

Top view drawing of a square integrated circuit package. The drawing includes the following dimensions and labels:

- Overall width:  $0.676 \pm 0.006$  (17.17  $\pm$  0.152) SQ
- Inner width:  $0.476 \pm 0.006$  (12.00  $\pm$  0.152) SQ
- Lead #1 IDENT: Points to a specific lead on the right side.
- UNIQUE CORNERS: Points to the corners of the package.
- Internal dimensions:
  - Width of the central square:  $0.190$  (4.978) TYP
  - Width of the inner square:  $0.392$
- Lead dimensions:
  - Lead width:  $0.048 \pm 0.003$
  - Lead thickness:  $-0.002$  DIA
  - Lead pitch:  $\pm 0.075$  DIA
  - Lead spacing:  $(1.188 - 0.051)$
  - 3 PLCS (NOT USED FOR LOCATING)

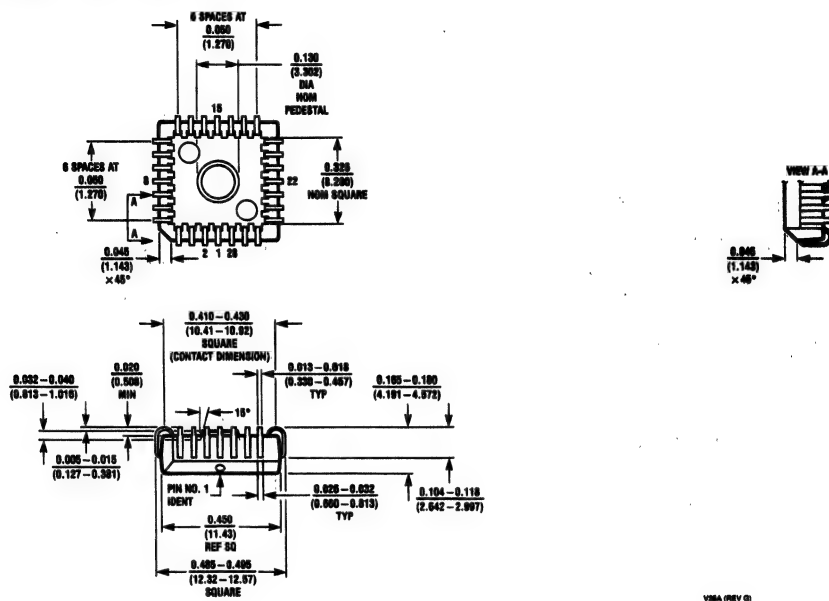
Technical drawing of a 16-pin DIP package. The top view shows a square body with pins on all four sides. Dimensions include: pin pitch 0.020 TYP (0.508), pin width 0.0086-0.0118 (0.2184-0.2987) TYP, body width 0.063 (1.548) 4x, and body length 0.0635 ± 0.0007 (0.0640 ± 0.0178). The side view shows a package height of 0.065 ± 0.004 (1.051 ± 0.102), a lead height of 0.040 (1.040), a lead thickness of 0.022 (0.560), a body thickness of 0.180 (4.572), and a lead angle of 0-4° TYP. The bottom view shows a lead width of 0.360 ± 0.006 (0.144 ± 0.152).

Figure 1: Pin Assignments for the 16-Pin DIP Package. The diagram shows a top view of a 16-pin DIP package with pins numbered 1 to 16. Dimensions are provided in inches and millimeters. Key dimensions include: Pin 1 to Pin 16 pitch: 0.385 (9.778) mm; Pin 1 to Pin 16 width: 0.060 (1.524) mm; Pin 1 to Pin 16 height: 0.193 (4.902) mm; Pin 1 to Pin 16 depth: 0.045 (1.143) mm; Pin 1 to Pin 16 length: 0.012 (0.305) mm; Pin 1 to Pin 16 width: 0.008 (0.203) mm.

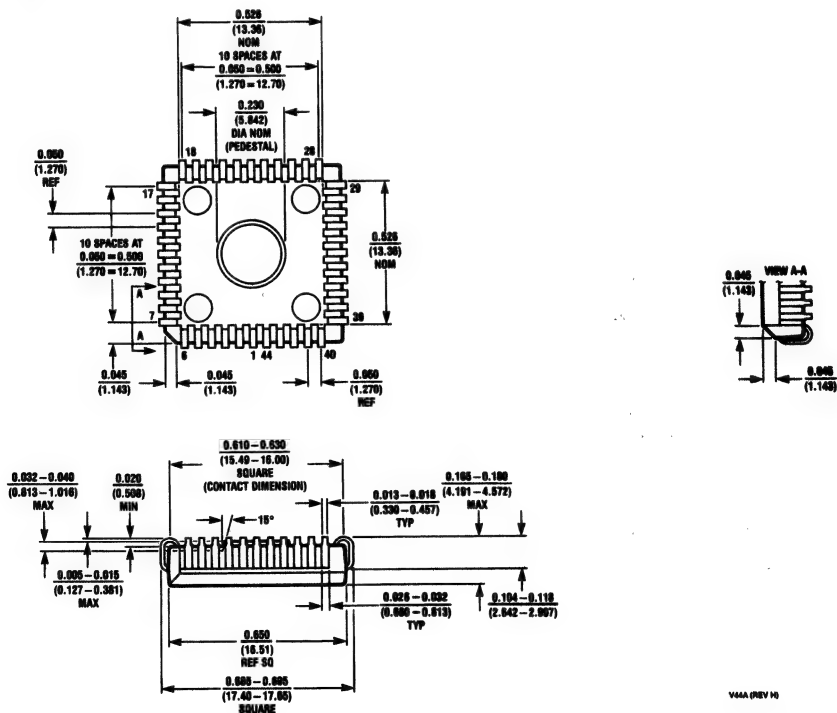
10



**28 Lead Plastic Chip Carrier (V)  
NS Package Number V28A**



**44 Lead Plastic Chip Carrier (V)**  
**NS Package Number V44A**









## NOTES



## NOTES



## NOTES